香港中文大學
The Chinese University of Hong Kong

CENG3430 Rapid Prototyping of Digital Systems

Special Arrangements for Online Teaching

Ming-Chang YANG

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CENG3430 Course Information

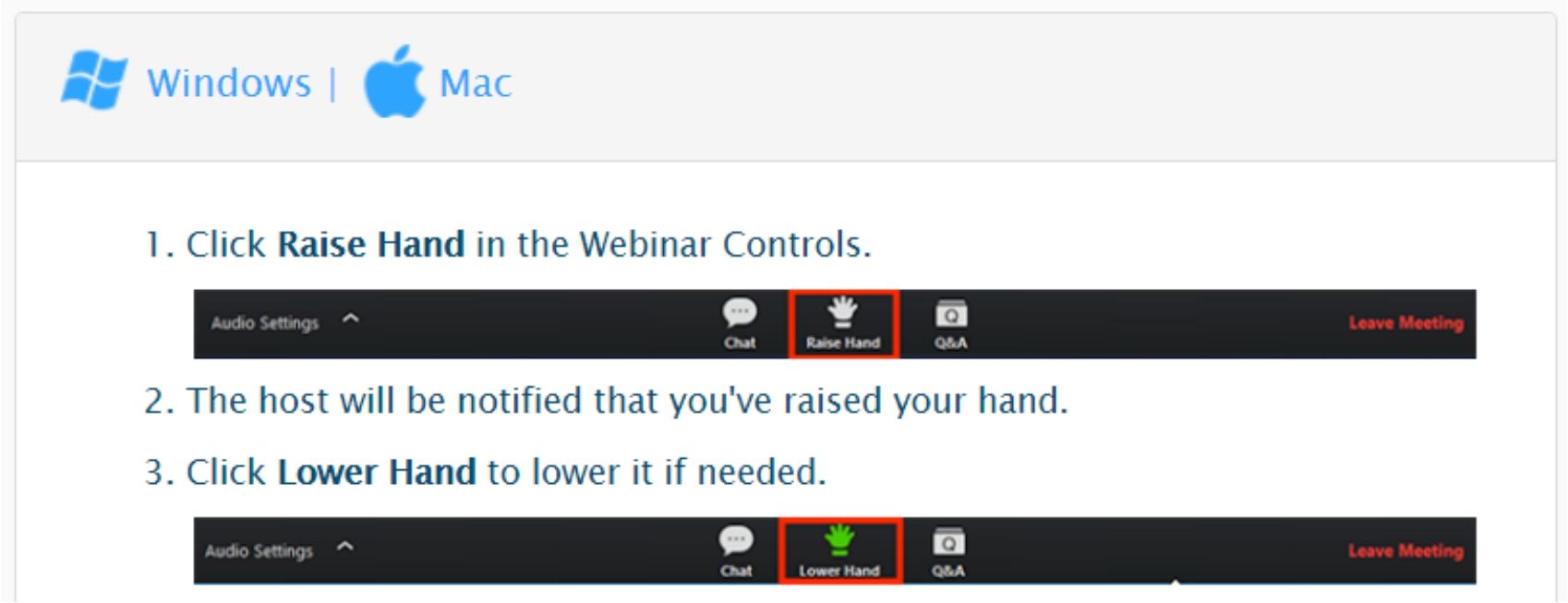
- **CENG3430 Rapid Prototyping of Digital Systems**
- **Course Time and Place**
  - **Lecture** (*2)
    - MON 16:30~18:15 (**ZOOM**)
  - **Lab** (*2)
    - TUE 16:30~18:15 (**ZOOM**)
  - **New: Online Q & A**
    - FRI 13:30~15:00 (**ZOOM**)

The recordings will be available at course website. (passwd: same as ZOOM)

- **Course Website**
  - http://www.cse.cuhk.edu.hk/~mcyang/ceng3430/2020S/ceng3430.html
  - https://blackboard.cuhk.edu.hk/

Tips: Raise Hand and In-meeting Chat

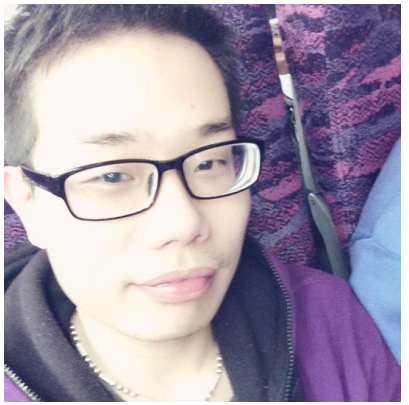
- To have good quality of online sessions, I will **mute everyone** by default.
- Questions? **Raise Hand** (before Unmute)



- Questions? **In-meeting Chat**

Course Instructor & Teaching Assistants

- **Course Instructor**
  - Prof. Ming-Chang YANG (楊明昌)
    - Office: SHB 906 (3943-8405)
    - Office Hours: *requested* ***by email***
    - Email: mcyang@cse.cuhk.edu.hk
- **Teaching Assistants**
  - Tinghuan CHEN (陳庭歡)
    - Office: SHB 905
    - Office Hours: FRI 13:30~15:00 (**ZOOM**)
    - Email: thchen@cse.cuhk.edu.hk
  - Guangliang YAO (姚廣亮)
    - Office: SHB 1026
    - Office Hours: FRI 13:30~15:00 (**ZOOM**)
    - Email: glyao@cse.cuhk.edu.hk



Course Assessment (w/ Final)

- Grading *(subject to changes)*
  - Class Exercises 10%
  - Laboratory Exercises 25%
  - Final Project 40%
  - Final Exam 25%
  - *Bonus* 5% (How to get? Q&A, Best Project)

- Notes
  - Lab. Exercises and Final Project: two students in a group
  - A student must attend at least 80% of lectures in order to gain all class attendance/exercise credits

New: Course Assessment (w/o Final)

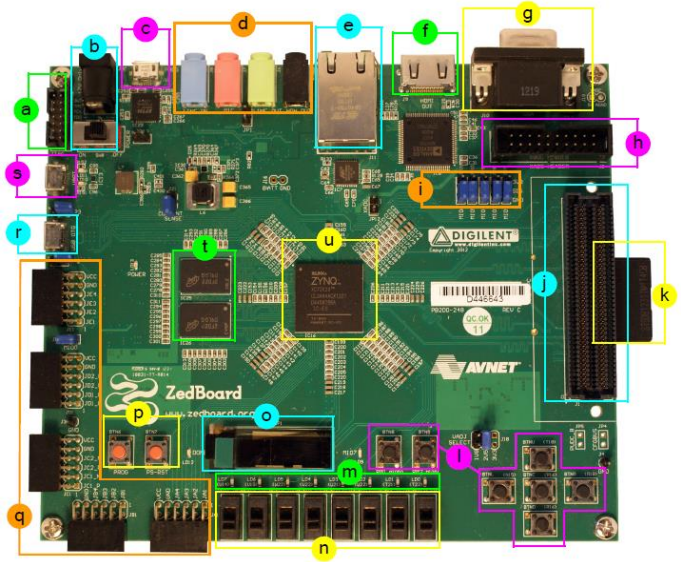
- Grading *(subject to changes)*
  - ~~Class Exercises 0%~~ (cancelled!)
  - Laboratory Exercises 40%
  - Final Project and Report 60%
  - ~~Final Exam 0%~~ (cancelled!)
  - Bonus 5%
- Notes
  - Lab. Exercises: **EVERY** student should submit individually
  - Final Project and Report: **1-2** students in a group
  - ~~A student must attend at least 80% of lectures in order to gain all class attendance/exercise credits.~~

New: Lab Arrangement

- **Software**: Vivado WebPACK™ Edition (link)
  - It is a FREE version of the design suite.
  - It supports Windows or Linux operating systems.
    - Need a NB? Loan from CUHK (Student Notebook Loan Scheme).

Application Deadline: 5:00 p.m., 17 Feb. 2020

- **Hardware**: Zynq ZedBoard
  - Dual-core ARM Cortex-A9, with Traditional FPGA
  - Extra accessories? Pick-up at CUHK or Local Mail



a Xilinx JTAG connector
b Power input and switch
c USB-JTAG (programming)
d Audio ports
e Ethernet port
f HDMI port (output)
g VGA port
h XADC header port
i Configuration jumpers
j FMC connector
k SD card (underside)
l User push buttons
m LEDs
n Switches
o OLED display
p Prog & reset push buttons
q 5 x Pmod connector ports
r USB-OTG peripheral port
s USB-UART port
t DDR3 memory
u Zynq device (+ heatsink)

New: Lab Assessment

- Every student must do all lab exercises **individually**.
- Attendance policy is **cancelled** for lab sessions.
  - The **20% demo bonus** is also **cancelled** for fairness.
  - During regular lab sessions, tutors will be online for Q & A.
  - One additional 90-minute online Q & A session will be held.
- **Source code(s)** and a **short demo video** must be submitted to blackboard for assessment.
  - Deadline: *before the next week lab sessions*
  - Late submissions? **NOT** acceptable (*or send us email for obtaining agreement before the regular deadline*)
- Every student will get one ZedBoard for practice.
  - Use it **CAREFULLY**, and **MUST** return at the end of term

New: CENG3430 Course Schedule

W	Date	Lecture	Lab
1	Jan 6, 7	Lec00: Course Information	No lab
2	Jan 13, 14	Lec01: Introduction to VHDL	Lab01: Vivado & Software Simulation
3	Jan 20, 21	Lec02: Introduction to ZedBoard	Lab02: First Program on ZedBoard
4	Jan 27, 28	Lunar New Year Vacation (No class)	No lab
5	Feb 17, 18	Lec03: Architectural Styles of VHDL	Lab03: 4-to-1 Multiplexer
6	Feb 24, 25	Lec04: Combinational & Sequential Circuit	Lab04: Serial-in-parallel-out Shift Register
7	Mar 2, 3	Lec05: Finite State Machine Lec06: Use of Clock and Pmod	Lab05: Driving Seven Segment Display
8	Mar 9, 10	Lec07: Driving VGA Display Lec08: Use of Signals and Variables	Lab06: Driving VGA Display
9	Mar 16, 17	Lec09: Integration of ARM and FGPA	Lab07: Software Stopwatch with ARM
10	Mar 23, 24	Lec10: Embedded Operating System	Lab08: Software Stopwatch with Linux
11	Mar 30, 31	Reading Week (No class)	No lab
12	Apr 6, 7	Lec11: High Level Synthesis	Lab09: High Level Synthesis Exercise
13	Apr 13, 14	Public Holiday – Easter (No class)	**Final Project Proposal (ZOOM)**
14	Apr 20, 21	Lec12: VHDL versus Verilog	Lab10: SIPO Shift Register in Verilog
15	Apr 27, 28	**Final Project Consultation (I)**	**Final Project Consultation (II)**
※	May 12	**Final Project Demonstration and Report Due**	